

# High-Efficiency Cells From Layer Transfer: A First Step Toward Thin-Film/Wafer Hybrid Silicon Technologies

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**Abstract**—Future low-cost Si photovoltaics shall combine the high-efficiency potential of ultrathin monocrystalline Si films with the low cost per area of the Si-thin-film photovoltaics. The literature describes various techniques for fabricating ultrathin monocrystalline Si films with no need for sawing wafers. Layer transfer using epitaxy on porous Si and subsequent layer separation is one option. We demonstrate an independently confirmed aperture efficiency of 19.1% for a 4-cm<sup>2</sup>-sized layer transfer cell with a thickness of 43 μm. This cell has a passivated emitter and rear contact structure with an Al<sub>2</sub>O<sub>3</sub>-surface passivation by atomic layer deposition and lasered contact openings. Highly efficient thin crystalline solar cells have to be integrated into modules. We also report on laser bonding of Si cells to a metalized carrier for module integration.

**Index Terms**—Aluminum oxide passivation, laser bonding, layer transfer, thin film/wafer hybrid.

## I. INTRODUCTION

MONOCRYSTALLINE Si has the key advantage of abundant availability. Crystalline Si champion wafer cells reached 24% on an industrial production line, and modules with wafer cells reached 20% efficiency [1]. This is the crystalline side of the “Si road.” On the other side, thin-film modules with amorphous and microcrystalline Si have the advantage of low processing costs per area. Significantly, less silicon is required, and the module fabrication is integrated. However, the highest confirmed stabilized cell efficiency is only 12.5% on 0.27 cm<sup>2</sup> [2], and record modules reached 10% [3]. This is only about half the efficiency of the crystalline cells and modules.

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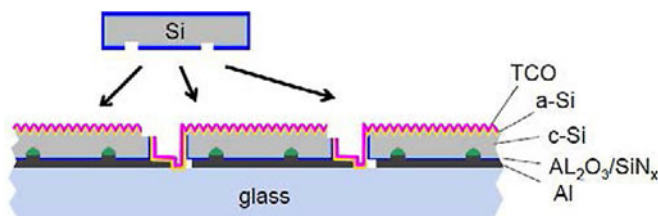


Fig. 1. Schematic representation of a hypothetical thin-film/wafer hybrid module concept employing an a-Si heterojunction. The interconnection of the thin-film cells is realized by transparent conductive oxide (TCO) deposition and laser scribing.

Today, crystalline Si photovoltaics is the technology that dominates the market. Past cost reductions in crystalline Si photovoltaics were mainly achieved by reducing the cost per area rather than by improving the power output per area. For crystalline Si, the reduction of cost per area will, in the long run, remain the key challenge due to the physical limitations of the cell efficiency that are coming close.

It is the Si thin-film world that demonstrates how low costs per area can be achieved. It is, therefore, our expectation that minimum photovoltaic system costs will not be realized on either of the two extreme sides of the “Si road”: complex processing of highly efficient modules here and low-efficiency modules of little complexity there. We rather foresee an attractive option for a hybrid technology employing thin monocrystalline Si films that are partly processed and interconnected by applying thin-film technologies. We term such approaches [4] thin-film/wafer Hybrid Si (HySi) technologies.

## II. VISIONARY THIN-FILM/WAFER HYBRID TECHNOLOGY

There are many HySi technologies of which one could think. Fig. 1 illustrates just one hypothetical example of the character of what is meant by a HySi module. For this example, we start with a rear-side metalization that is sputtered or evaporated onto a large carrier, e.g., glass, and then structured by laser scribing. Thin monocrystalline Si films (<50 μm) are passivated on one or both sides. A laser opens the dielectric layer to contact the base. The films are then connected to the rear metalization in a mechanically stable and electrically conducting manner. The surface of all cells is then textured in a large area process, e.g., by plasma etching. A large-area plasma process forms a heterojunction. The interconnection shall be realized by depositing a transparent conducting oxide (TCO) and subsequent laser scribing.

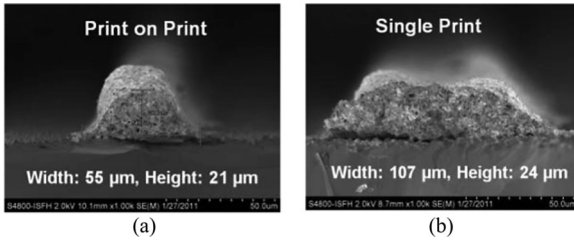


Fig. 2. Cross-sectional scanning electron micrographs of silver front contact fingers after firing on fully processed solar cells applying (a) PoP screen printing with a finger width of 55  $\mu\text{m}$  and (b) standard single printing with a finger width of 107  $\mu\text{m}$ .

Small cells would be advantageous to get along with a low-TCO sheet resistance and without the need to apply metal fingers. Small cells would also reduce the mechanical stress during thermal cycling.

### III. STEPS TOWARD THIN-FILM/WAFER HYBRID SI CONCEPTS

At the Institute for Solar Energy Research Hamelin (ISFH), Emmerthal, Germany, it is our plan to gradually convert current Si cell technologies into a thin-film/wafer HySi module. Such a gradual development has the advantage that some steps toward HySi modules may already be applied to conventional wafer technologies before the—admittedly very ambitious—HySi technology is ready to be transferred to industry. In this paper, we describe some steps that ISFH has already taken toward the HySi technology. For a gradual change from conventional wafers to HySi modules, we first require a state-of-the-art standard screen-printing technology as a starting point. Please note that a screen-printed metalization could possibly also be considered for “gluing” thin Si films to thermally matched glass carriers. This has already been reported in 2005 [5], [6].

#### A. Step 1: Develop a State-of-the-Art Baseline Screen-Printing Process for Monocrystalline Si.

Fig. 2 shows that a front-side print-on-print (PoP) process reduces the Ag finger width from about 100  $\mu\text{m}$  to below 70  $\mu\text{m}$ . With a full-area aluminum back-surface field (BSF), a homogeneously doped emitter, and PoP, we achieve an independently confirmed AM1.5G efficiency of 18.7% on p-type Czochralski (Cz)–Si wafers with an area of 125 mm  $\times$  125 mm [7]. The other parameters of the  $J$ – $V$  curve are listed in Table I.

#### B. Step 2: Develop a Mass-Produced Improved Rear Passivation that is Temperature Stable

Surface passivation is necessary since the HySi modules will contain very thin Si wafers that are sensitive to surface recombination. A high-temperature stable passivation scheme allows for a wider temperature range of subsequent processing steps, which is also applicable to screen-printed cells, and is therefore to be preferred. At ISFH, we selected  $\text{Al}_2\text{O}_3$  for rear-side passivation [8]–[10]. We developed the laser contact-opening (LCO)-technique using laser pulses with a length of some picoseconds [11] to generate a passivated emitter and rear contact

TABLE I  
PARAMETERS OF CURRENT–VOLTAGE CURVES UNDER 0.1 W/ $\text{cm}^2$  OF AM1.5-GLOBAL ILLUMINATION AT 25  $^\circ\text{C}$

	A	t	$\eta$	FF	$V_{\text{OC}}$	$J_{\text{SC}}$
Step: Process, Material	[ $\text{cm}^2$ ]	[ $\mu\text{m}$ ]	[%]	[%]	[mV]	[ $\text{mAcm}^{-2}$ ]
Step 1: Scr. pr. full BSF, Cz-wafer	146	170	18.7*	79.8	632	37.1
Step 2: Scr. pr. PERC $\text{Al}_2\text{O}_3$ , Cz-wafer	149	180	19.0*	75.1	652	38.9
Step 3: Evap. PERC $\text{Al}_2\text{O}_3$ , FZ-wafer	4.00	275	21.7*	79.9	673	40.3
Step 4: Evap. PERC $\text{Al}_2\text{O}_3$ , PSI process	3.98	43	19.1*	77.6	650	37.8

Abbreviations Used: Cell Area  $A$ , Si Thickness  $t$ , Efficiency  $\eta$ , Fill Factor FF, Open-Circuit Voltage  $V_{\text{OC}}$ , and Short-Circuit Current Density  $J_{\text{SC}}$ .

The metalization is either screen printing (scr. pr.) or evaporation (evap.).

\*Independently confirmed by Fraunhofer ISE CalLab.

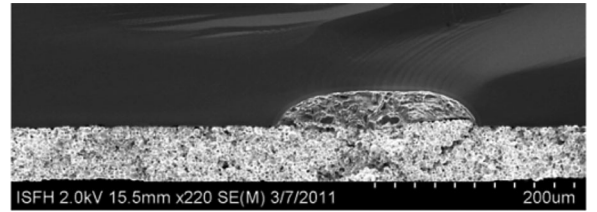


Fig. 3. Cross-sectional scanning electron micrograph of a screen-printed,  $\text{Al}_2\text{O}_3/\text{SiN}_x$  rear-side-passivated PERC solar cell with local line contacts formed by LCO and Al screen printing on the rear side.

(PERC) [12] structure. Using a Cz–Si wafer,  $\text{Al}_2\text{O}_3/\text{SiN}_x$  rear-side passivation, LCO, and screen printing on both sides, we achieve a confirmed efficiency of 19.0% [13]. The other data of the  $J$ – $V$  curve are listed in Table I.

Fig. 3 shows a cross-sectional scanning electron micrograph of a rear-passivated screen-printed solar cell. A particular challenge for such a cell type is the formation of a local aluminum rear contact that is void free and forms a uniform BSF layer with a low rear surface recombination velocity. Recent investigations show that the aluminum screen-printing paste [14], as well as the contact geometries [15], strongly influences the BSF formation. Dynamic infrared lifetime mapping (dyn-ILM) [16] is capable of measuring carrier lifetimes in fully metalized Si wafers [17]. With this technique, we find a recombination velocity of  $S_{\text{pass}} = 8 \text{ cm/s}$  ( $J_{\text{pass}} = 10 \text{ fA/cm}^2$ ) at the passivating interface and a diode saturation current density of  $J_{\text{cont}} = 1 \times 10^4 \text{ fA/cm}^2$  at the local contacts.

#### C. Step 3: Replacing Screen Printing by Vacuum Deposition

Thin-film technologies apply physical vapor deposition for metalization and are not compatible with temperatures above 800  $^\circ\text{C}$  as they are typically used for firing screen-printing pastes. At ISFH, we investigate Al evaporation as an alternative metalization process, since it creates little damage to the crystalline Si and high deposition rates are feasible. We set up an

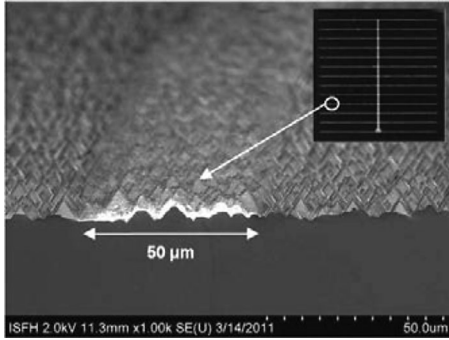


Fig. 4. Scanning electron micrograph of an in-line-evaporated front grid. The evaporated Al-layer is 50  $\mu\text{m}$  wide. The inset shows a photo of the full grid covering a cell area of 2 cm  $\times$  2 cm.

in-line evaporation system ATON 500 (Applied Materials) [18]. Although the visionary HySi module mentioned earlier would not require a front grid, we nevertheless investigate options for structured evaporations with our in-line tool. For evaporating finger grids, we use  $(700 \pm 10)$ - $\mu\text{m}$ -thick silicon shadow masks for the in-line evaporation of the aluminum front grid. The masks are fabricated by a laser processing and subsequent anisotropic etching [19]. Fig. 4 shows the scanning electron micrograph of an evaporated finger that has a width of 50  $\mu\text{m}$ . On average, the fingers are  $(60 \pm 20)$   $\mu\text{m}$  wide. The thickness of the fingers shall be improved by changing the geometry of the mask [19]. The high thermal mass of the silicon shadow mask allows a high local aluminum deposition rate. The estimated throughput is 1200 wafers/h for a wafer of 156 mm  $\times$  156 mm using an ATON 1600 system (Applied Materials) and 15- $\mu\text{m}$ -thick fingers of 50  $\mu\text{m}$  width in a cell design with three bus bars.

For the cell fabrication, we keep the PERC design and the  $\text{Al}_2\text{O}_3$  passivation of Step 2 but apply Al evaporation instead of screen printing. On 4- $\text{cm}^2$ -large crystalline float-zone Si solar cells, atomic layer deposited (ALD) aluminum oxide passivates both surfaces. On the emitter, two ALD cycles generate an  $\text{AlO}_x$  tunneling barrier to enhance the temperature stability and to passivate the emitter. The rear side receives an  $\text{Al}_2\text{O}_3/\text{SiN}_x$  stack. Local contacts on the back side are defined by LCO. Al is evaporated to the rear side. With this device structure, we achieve an independently confirmed efficiency of 21.7% [20]. The open circuit voltage  $V_{oc}$  is 673 mV. See Table I for the other data. The tunneling oxide underneath the front-size grid improves the cell voltage by 12 mV when compared with a cell that is processed without that layer [20]. The  $\text{AlO}_x$  layer does not, however, improve the passivation on the nonmetalized surface.

#### D. Step 4: Saving Si Material by Using Thin Crystalline Si Layers

To this end, we develop the so-called porous Si (PSI) process that employs epitaxial growth on PSI. The epitaxial film is subsequently separated from the growth substrate. Layer transfer reduces the  $>120$ - $\mu\text{m}$  kerf loss of wafer sawing to about 10  $\mu\text{m}$  of Si loss due to surface conditioning that is required prior to the epitaxy. In addition, the epitaxial cell thickness is only 5 to

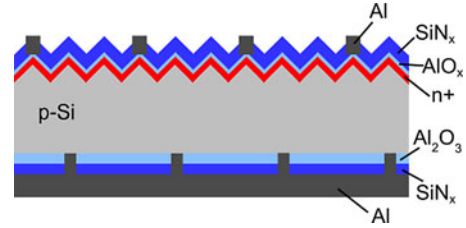


Fig. 5. Cell structure used in Step 3 and Step 4. The rear side is passivated by an  $\text{Al}_2\text{O}_3/\text{SiN}_x$  double layer. The Al is evaporated on both sides using a laboratory evaporator (BAK 600).

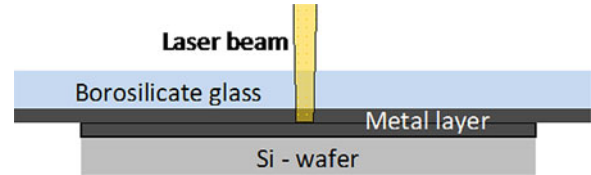


Fig. 6. Schematics of the laser bonding process.

50  $\mu\text{m}$  and, thus, is less than the conventional wafer thickness of 180  $\mu\text{m}$ . Both effects together reduce the Si consumed per cell area by a factor of 5 to 20. Epitaxy from the gas phase replaces the CVD process of the Siemens process. Block casting or ingot growth and poly-Si feed stock is only required for the growth substrate. Boron-doped epitaxial cells do not suffer from the B-O complex if oxygen is excluded from the epitaxial layer. We successfully run the PSI process with the PERC cell structure developed in Step 3 [21] (see Fig. 5). These results will be presented in the final section of this paper.

#### E. Step 5: Integrating the Thin-Film Cells Into Modules

Any HySi technology approach requires the attachment of monocrystalline Si films to the module carrier. This attachment may be done at a high or at a low temperature and could possibly be combined with the formation of the local contacts.

High-temperature bonding of Si to glass has already been demonstrated [5], [6]. These authors showed that rapid thermal annealing of an Si/Al/glass stack simultaneously bonds the Si to the glass and forms a BSF layer. An efficiency of 14.8% was reported for a 60- $\mu\text{m}$ -thick Si layer [22]. The simultaneous bonding to glass and formation of local BSF layers was not yet demonstrated. Such approaches require a high-temperature stable glass or carrier.

Fig. 6 shows the schematics of direct laser bonding of Al-coated wafers to an Al-coated glass substrate. This approach does not require a high-temperature stable glass. Here, we report on our first experiments on laser bonding glass to Si. The sample size is 4.9  $\text{cm}^2$ . The Al metalization on the damage-etched Si wafer is 20  $\mu\text{m}$  thick. The glass (Borofloat, Schott) is coated with Al of thickness  $d$ . We apply eight pulses per bonding point with a wavelength of 355 nm, a pulselength of 20 ns, and a pulse energy of 176  $\mu\text{J}$ . A fraction of 1% of the sample area is laser bonded, and then, we tear off the Si from the glass by pulling normally with a tensile testing machine. Inspection of

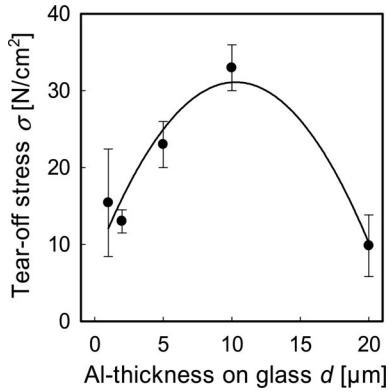


Fig. 7. Measured tear-off stress of an Si wafer metalized with  $20\ \mu\text{m}$  Al. A fraction of 1% is laser bonded. The line is a guide to the eye.

the teared-off samples by scanning electron microscopy reveals a bonding point diameter of  $(60 \pm 20)\ \mu\text{m}$ .

Fig. 7 shows the results of the tear-off experiments. The strength of the bonding increases with the aluminum layer thickness up to  $d = 10\ \mu\text{m}$ . The maximum tear-off stress is  $\sigma = (33 \pm 3)\ \text{N}/\text{cm}^2$ . The strength decreases with thickness for  $d > 10\ \mu\text{m}$ . We explain this as follows: A gap of a few micrometers exists between the wafer and the glass due to not the perfectly plane surface of the Si wafer. For bonding, molten Al is required to bridge this gap. With increasing layer thickness  $d$ , larger amounts of Al are available, and the strength of the bond, therefore, increases. When the thickness  $d$  increases to values beyond  $10\ \mu\text{m}$ , the pulse energy becomes insufficient to melt the Al at the interface. The bonding strength decreases. We also analyze possible defect generation during bonding by measuring lifetimes with the dyn-ILM technique [15] before and after bonding. For this, we use a  $10\text{-}\mu\text{m}$ -thick Al layer on glass. The effective carrier lifetimes are  $(1810 \pm 60)$  and  $(1770 \pm 80)\ \mu\text{s}$  before and after laser bonding. This demonstrates the absence of laser damage. Tests on the thermally cycling stability of laser bonding with Al will be presented elsewhere [23].

#### IV. LAYER TRANSFER CELL WITH RECORD EFFICIENCY

Shortly after the introduction of the layer transfer process with PSI [24], [25], a cell efficiency of 12.5% was demonstrated by Tayanaka *et al.* [26] and was then gradually increased by various groups. In 2009, Reuter *et al.* reported an independently confirmed efficiency record of 16.9% for a layer transfer cell glued to glass [27]. The area of the cell was  $2.0\ \text{cm}^2$ . These authors found that gluing the layer to the glass comes along with light absorption in their glue. They processed a transfer cell without gluing it to a superstrate and reached an in-house-measured efficiency of 17.0% on an area of  $1.1\ \text{cm}^2$  [27]. Since then, no further efficiency improvements for layer-transfer cells on PSI are reported in the literature.

##### A. Thin-Film Generation

Fig. 8 shows the process of generating thin monocrystalline Si wafers using layer transfer with PSI (PSI process). We start with a highly doped Cz-grown, p-type substrate wafer of 6 inches in

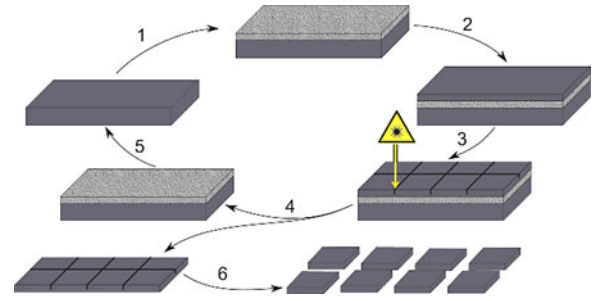


Fig. 8. Cyclic layer transfer. (Step 1) A substrate wafer receives a PSI surface. (Step 2) An epitaxial layer grows on the porous surface. (Step 3) Laser scribing down to half the layer thickness. (Step 4) Liftoff. (Step 5) Etching off residual PSI wafer reuse. (Step 6) Cleaving the EPI layer into single cells for device processing.

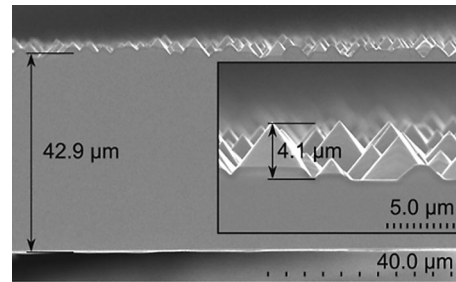


Fig. 9. Scanning electron micrograph of a cross section of the epitaxial layer after separation from the substrate wafer. (Inset) Surface texture, enlarged.

diameter that receives a porous double layer by electrochemical etching. During a high-temperature annealing in a hydrogen atmosphere, the surface reorganizes and then serves as a seed layer for the epitaxial growth of a B-doped layer ( $0.5\ \Omega\cdot\text{cm}$ ) by atmospheric pressure chemical vapor deposition. Details were published elsewhere [21], [28]. We laser structure 14 pieces of  $2.5\ \text{cm} \times 2.5\ \text{cm}$  each from the 6-in epitaxial layer prior to liftoff. The residual PSI sticking to the samples is etched off. The front side receives a surface texture, while the other side is covered with a protective layer. Fig. 9 shows a cross-sectional scanning electron micrograph of one of the samples. The device thickness is  $(43 \pm 2)\ \mu\text{m}$ .

##### B. Cell Process

We diffuse a phosphorus emitter with a sheet resistance of  $100\ \Omega/\text{sq}$  from a  $\text{POCl}_3$  source and passivate the rear side with  $30\ \text{nm}$  of  $\text{Al}_2\text{O}_3$  that we deposit in a commercial ALD reactor (FlexAl, Oxford Instruments, Oxfordshire, U.K.). Then, a  $100\text{-nm}$ -thick plasma-enhanced chemical vapor deposition  $\text{SiN}_x$  capping layer [29] is deposited in a parallel-plate reactor (Plasmalab 80+, Oxford Instruments). The back-side passivation is locally opened by a laser (SuperRapid, Lumera, 9-ps pulselength) for contacting. We ablate contact pads with a square pattern and an areal coverage of 4–5%. The opened back side is subsequently metalized by electron gun evaporation of Al. Atomic layer deposition forms a nominally  $0.24\text{-nm}$ -thick  $\text{AlO}_x$  tunneling layer on the entire emitter surface. This layer also acts as a contact passivation and enhances the temperature stability of the emitter contact. We define the front-side grid by

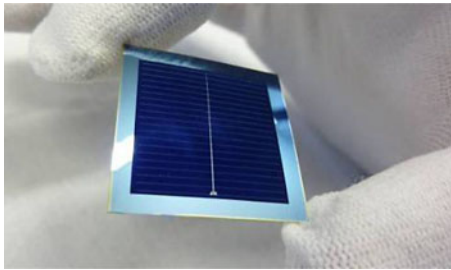


Fig. 10. Forty-three-micrometer-thick solar cell with evaporated Al contacts. The cell area is  $2 \text{ cm} \times 2 \text{ cm}$ .

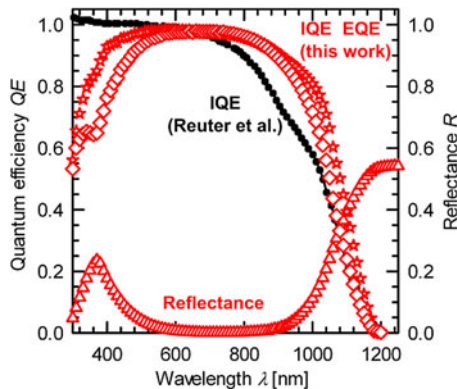


Fig. 11. Internal (stars) and external (diamonds) quantum efficiency and hemispherical reflectance (triangles) of the PSI cell. The IQE of the 17.0%-efficient free-standing cell by Reuter *et al.* (black dots, data from [27]) is shown for reference purposes.

evaporation of Al through a shadow mask. An  $\text{SiN}_x$  double layer passivates the emitter and functions as an antireflection coating. Annealing the cell in air on a hot-plate finishes the process. More details on the process are given in [21].

### C. Device Results

Fig. 10 shows a photo of a finished cell. The parameters of the illuminated current–voltage curve as measured by ISE CalLab for an AM1.5G spectrum at  $0.1 \text{ W/cm}^2$  and  $25^\circ\text{C}$  are listed in Table I. The independently confirmed aperture efficiency is  $(19.1 \pm 0.4)\%$  and is, thus, 2% absolute higher than the previous record transfer cell. This is the highest efficiency reported so far for a layer transfer Si cell. It is also the highest efficiency for any epitaxial thin-film cell that did not consume a wafer.

Fig. 11 shows the external quantum efficiency (EQE) (diamonds), reflectance (R) (triangles), and the internal quantum efficiency (IQE) (stars) of our device and compares it with the IQE (dots) of the previous record cell by Reuter *et al.* [27]. Our cell has further potential for improvements in the short-wavelength range.

Although the layer transfer cell process demonstrated here is certainly too complex for mass production, and although the integration of such cells into an integrated module still needs to be demonstrated, we consider the record efficiency reported here as an encouraging step toward thin-film/wafer Si hybrid modules.

TABLE II  
PARAMETERS OF THE DEVICE SIMULATION

Symbol	Value	Type	Ref
<i>Bulk properties</i>			
$\tau_{n0}$	20 $\mu\text{s}$	f	
$\tau_{p0}$	65 $\mu\text{s}$	f	
<i>Surface properties</i>			
$J_{0,f}$	(230 $\pm$ 80) $\text{fA/cm}^2$	w	
$R_f$	100 $\Omega$	f	
$J_{0,fc}$	800 $\text{fA/cm}^2$	e	
$R_{fc}$	1.5 $\text{m}\Omega$	e	
$J_{0,b}$	1 $\text{fA/cm}^2$	w	
$J_{0,bc}$	3000 $\text{fA/cm}^2$	w	[33]
$R_{bc}$	1.5 $\text{m}\Omega$	e	
<i>Contact resistances for network simulation</i>			
$R_{front}$	7 $\text{m}\Omega\text{cm}^2$	e	
$R_{back}$	3 $\text{m}\Omega\text{cm}^2$	e	

Capture times  $\tau_{n0}$  and  $\tau_{p0}$  in the bulk. The saturation current density is  $J_{0,f}$  at the passivated emitter,  $J_{0,fc}$  at the contacted emitter,  $J_{0,b}$  at the passivated back side, and  $J_{0,bc}$  at the contacted back side.  $R_f$ ,  $R_{fc}$ , and  $R_{bc}$  are the corresponding sheet resistances. For a network simulation, we use the contact resistance  $R_{front}$  and  $R_{back}$ , respectively. Type indicates data directly measured on epitaxial films (f), data measured on wafers (w), or estimated data (e).

### D. Free Energy Loss Rate Analysis

We perform a free energy loss analysis [30] in combination with transport modeling [31], [32] to quantify the loss channels.

We first determine the bulk lifetimes by surface passivating the samples and measuring the injection dependent lifetime with a quasi-steady-state photoconductance lifetime tester. The passivating dielectric is  $\text{Al}_2\text{O}_3$  deposited by atomic layer deposition. We take the low injection lifetime as the minority carrier capture time  $\tau_{n0}$ . The high injection lifetime minus the low injection value is the majority carrier capture time  $\tau_{p0}$ . At all injection levels, the lifetime exceeds 20  $\mu\text{s}$ .

Next, we measure the diode saturation current densities and the sheet resistances of all surface regions of the PSI cell. Table II lists the input parameters. Where a direct measurement is not available, we use data generated with similar process parameters on wafers or estimated data.

Fig. 12 shows the simulated free energy loss rates of the PSI cell (43  $\mu\text{m}$ ) for the most important loss channels. All other parameters are kept constant when varying the thickness from 43  $\mu\text{m}$  down to 30 and 20  $\mu\text{m}$ . The largest loss rates are due to recombination in the emitter and at the nonpassivated back contacts. These losses amount to 47% of the total losses (24% emitter and 23% back contacts). The other contributions are Shockley–Read–Hall recombination in the base (17%), transport of holes in the base (16%), transport of electrons in the base (12%), and transport of electrons in the emitter (6%). The increase of the hole transport losses with decreasing thickness shown in Fig. 12 reveals that it is mainly lateral transport that causes the losses. In contrast, the transport loss of diffusing electrons is mainly caused by transport in the direction perpendicular to the cell surface and, thus, decreases with decreasing device thickness. The latter is linked to the large recombination at the metal contacts that cause a strong gradient of the carrier concentration toward the back side of the cell.

Measures to enhance the cell efficiency are, therefore, an improvement of the emitter and the introduction of a back

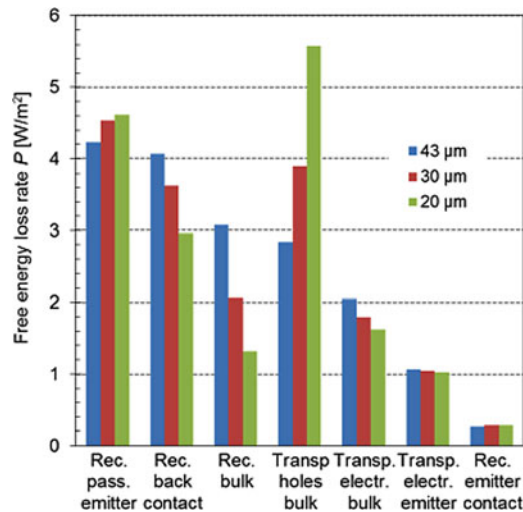


Fig. 12. Free energy loss rate analysis of the experimental PSI cell (43  $\mu\text{m}$ ) in comparison with thinner cells (30 and 20  $\mu\text{m}$ ). Losses are given at the maximum power point. A loss rate of 10  $\text{W}/\text{m}^2$  corresponds to an absolute efficiency loss of 1%.

surface field layer. The simulated PSI cell has an efficiency of 20.2%, a fill factor of 83.2%, and an open-circuit voltage of 642 mV. Obviously, this aforementioned simulation does not account for losses due to contact resistances and due to Joule heating in the evaporated metal fingers. Therefore, we combine the CoBo simulation with a network simulation using Linear Technology–Simulation Program with Integrated Circuit Emphasis (LT–SPICE) [34]. This network simulation does not change the simulated open-circuit voltage but reduces the simulated fill factor to 78.9% and the efficiency to the experimentally measured value of 19.1%. The efficiency drop from 20.2% to 19.1% corresponds to a free energy loss rate of 11  $\text{W}/\text{m}^2$  and is, thus, even larger than the losses due to emitter and back-contact recombination. Although the simulated efficiency agrees with the experiment, the simulated open-circuit voltage is 8 mV too small, and the simulated fill factor is 1.3% too large. This might partly be due to the two-dimensionality of our simulation that does not account for the 3-D current crowding at the local contacts. Three-dimensional CoBo simulations are planned to clarify this. It is also possible that the  $J_{o,bc}$  value that we measured on wafers is larger than that on the epitaxial cell due to autodiffusion of a weak BSF layer during epitaxy.

## V. SUMMARY

This paper is a written version of the presentation held at the 37th IEEE Photovoltaic Specialists Conference in Seattle, WA, and discusses thin-film/wafer HySi modules as a possible future option for low-cost Si photovoltaics. This paper reviews various recent result of the research at ISFH that is directed toward HySi modules. As one milestone of this study, we presented a confirmed world-record efficiency for a layer transferred laboratory cell. The efficiency is 19.1%, and the cell area is 4  $\text{cm}^2$ . Surface passivation is realized by ALD aluminum oxide. The emitter contact is also passivated by a tunneling aluminum oxide layer. The cell has evaporated Al contacts on both sides. As a first step

toward module integration of Al-contacted layer transfer cells, we report on direct laser bonding of Si cells to Al-metalized carriers. With a glass carrier, we reach a tear-off stress of 33  $\text{N}/\text{cm}^2$  with only one 1% of the cell area being bonded to the glass.

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