

# EFFECT OF SiO<sub>2</sub> THICKNESSES IN THERMAL-SiO<sub>2</sub>/PECVD-SiN STACKS ON SURFACE PASSIVATION OF *n*-TYPE Cz SILICON SUBSTRATES

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## ABSTRACT

The influence of SiO<sub>2</sub> thicknesses in thermal-SiO<sub>2</sub>/PECVD-SiN stacks on surface passivation of 2.5 Ωcm *n*-type Czochralski silicon substrates has been investigated. By annealing these stacks in air we achieve surface recombination velocities (SRV) better (i.e. lower) than 2.6 cm/s for thin SiO<sub>2</sub> layers. We find a clear correlation between the thickness of the oxide layers and the annealing duration for obtaining optimum surface passivation. Furthermore, we also show that the absolute passivation quality of the SiO<sub>2</sub>/SiN stacks correlates to the SiO<sub>2</sub> thickness. We find that the SRV increases with increasing oxide thickness. We also present data of the surface passivation of these SiO<sub>2</sub>/SiN stacks after storage in the dark for several months. We find a slight degradation of the surface passivation for thicker oxides and no observable degradation for the 10 nm thick SiO<sub>2</sub> layer in our SiO<sub>2</sub>/SiN stacks after 6 weeks of storage. Short annealing at 400°C in air restores the passivation quality and from then on remains unchanged for the measured storage time of 35 weeks.

## INTRODUCTION

Thermally grown oxide is the state-of-the-art surface passivation layer for *c*-Si. It passivates the surfaces efficiently for essentially all phosphorus-doping levels of practical relevance and also provides good surface passivation for *p*-type wafers for a wide range of substrate resistivities. A prominent example of SiO<sub>2</sub> surface passivation is given by the world-record solar cell efficiency of the *passivated-emitter and rear locally-diffused* (PERL) *c*-Si solar cell [1]. The surface passivation of the as-grown thermal oxide is moderate, but is significantly improved by a subsequent annealing in forming gas (H<sub>2</sub> in N<sub>2</sub>) [2] or upon depositing a hydrogen-rich silicon nitride (SiN) layer onto the oxidised surface [3]. However, the best results ( $S_{\text{eff}} \leq 2.4$  and 11.8 cm/s on *n*- and *p*-type FZ *c*-Si, respectively) are obtained by the so-called *alnear* scheme [4], where a layer of Al is evaporated onto the SiO<sub>2</sub> film prior to annealing at approximately 400°C. The aluminium oxidises residual H<sub>2</sub>O molecules in the SiO<sub>2</sub>, which releases atomic hydrogen that eventually saturates dangling bonds at the Si/SiO<sub>2</sub> interface. In this work we show that the oxide thicknesses in thermal-SiO<sub>2</sub>/PECVD-SiN stack systems exhibit a clear correlation to the achievable surface passivation as well

as to the required annealing time for obtaining optimal passivation. We show that thin oxides (< 40 nm) prove to be favourable for the Si surface passivation properties of these stacks. This finding is contrary to the observation of alnealed thermal SiO<sub>2</sub> layers, where residual water molecules in the SiO<sub>2</sub> layer are the source of the atomic hydrogen that passivates the Si/SiO<sub>2</sub> interface state density. We achieve with our SiO<sub>2</sub>/SiN stacks a surface recombination velocity of less than 2.4 cm/s, which shows a similar level of surface passivation as alnealed thermal oxide on moderately doped *n*-type silicon. We furthermore show that the SiO<sub>2</sub>/SiN stack systems provide a very stable surface passivation that does not degrade appreciably with time. The stability is most pronounced for stacks with thin SiO<sub>2</sub> layers.

## EXPERIMENTAL RESULTS

### Preparation of experiment

We use (100)-oriented Cz *n*-type silicon of 2.5 Ωcm resistivity and a thickness of 150-160 μm after saw-damage etching in KOH. Subsequently, the wafers were cleaned using the standard RCA procedure prior to oxidation in a cleaned quartz furnace tube at high temperatures. The SiO<sub>2</sub> thickness was varied by using different oxidation times and different growth temperatures. The first set of wafers was oxidized in dry O<sub>2</sub> at 900 °C for 15 min and has 10 nm grown oxide thickness. The second and third sets of wafers were oxidized in wet O<sub>2</sub>/H<sub>2</sub> ambient at 900 °C for 12 min (40 nm oxide thickness) and 185 min (270 nm oxide thickness), respectively. For the fourth set of wafers, the thermal oxide is grown at 1000 °C in wet O<sub>2</sub>/H<sub>2</sub> ambient for 65 min to a thickness of 330 nm. It is known that the as-grown oxides give a very poor surface passivation and an increase in passivation quality can be observed after PECVD-SiN deposition [3]. We have deposited 70 nm thick SiN films (for all sets of wafers) onto both wafer surfaces with a substrate temperature of 400 °C in a *remote* plasma-enhanced chemical vapour deposition (PECVD) system. Subsequently we annealed the wafers in ambient air at 400 °C on a hotplate for up to 30 min.

The effective lifetime  $\tau_{\text{eff}}$  was measured by the quasi steady-state photoconductance and transient photoconductance decay techniques [5]. Both methods show excellent agreement in lifetime measurements. We quantify the upper level of the effective SRV  $S_{\text{eff,max}}$  by

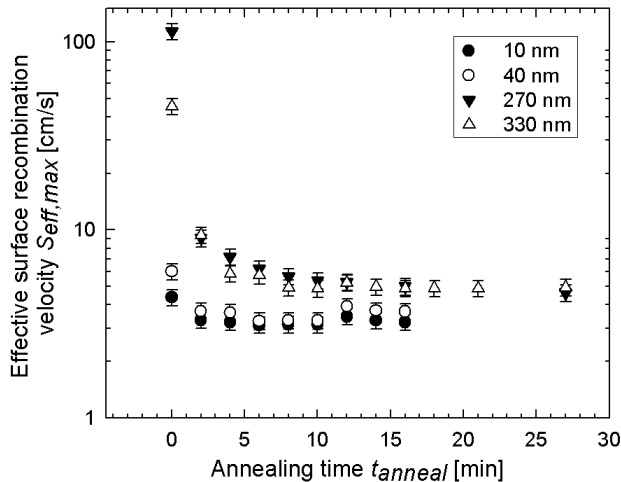
assuming infinite bulk lifetime and calculate  $S_{eff,max}$  from [6]:

$$S_{eff,max} \leq W / (2 \cdot \tau_{eff}) \quad (1)$$

where  $W$  is the wafer thickness.

### Annealing of SiO<sub>2</sub>/SiN stacks

Figure 1 shows the effect of SiO<sub>2</sub> thicknesses and subsequent thermal annealing on the effective SRV for surfaces passivated by thermal-SiO<sub>2</sub>/PECVD-SiN stacks. The presented data are averaged over 5-10 wafers for four different stack systems, which differ by the thickness of the thermal oxide. As can be seen from Figure 1, the “as-fabricated” (0 min of annealing time) SiO<sub>2</sub>/SiN passivation quality depends on the thickness of the thermal oxide between the Si wafer and the SiN coating: The passivation quality increases with decreasing the oxide thickness between Si-surface and SiN film. In order to benefit from the hydrogen passivation at the Si/SiO<sub>2</sub> interface, the hydrogen has to be transported from the SiN towards this Si/SiO<sub>2</sub> interface. In our experiments, the hydrogen transport and interface passivation is activated during the annealing step at 400°C. Our best values for the effective lifetimes measured at an excess carrier density of  $\Delta n = 10^{15} \text{ cm}^{-3}$  correspond to  $S_{eff}$  values less than 2.4 cm/s for 10nm oxide, 2.7 cm/s for 40nm oxide, 3 cm/s for 270nm oxide and 3.1 cm/s for 330nm oxide thickness. To our knowledge, these are the best  $S_{eff,max}$  values reported for 2.5 Ωcm *n*-type Cz crystalline silicon passivated by thermal-SiO<sub>2</sub>/PECVD-SiN stacks.

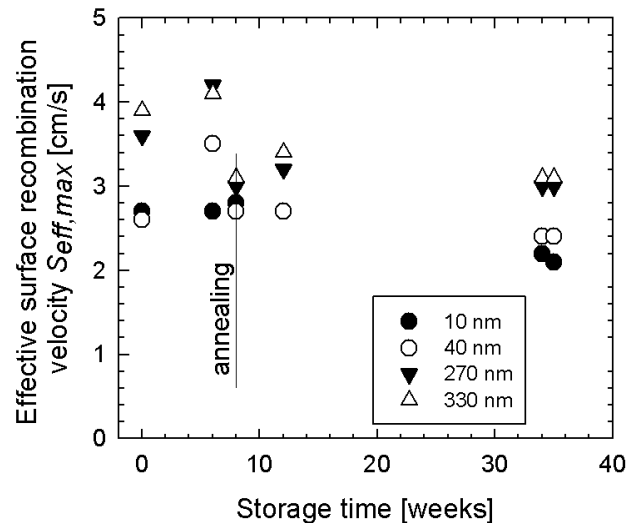


**Figure 1** Effective SRV, measured at injection level  $\Delta n = 1 \cdot 10^{15} \text{ cm}^{-3}$ , versus annealing time in air at 400 °C for *n*-type CZ silicon wafers (2.5 Ωcm) passivated with thermal-SiO<sub>2</sub>/PECVD-SiN stack. Different curves correspond to the different thicknesses of thermal oxide layer (10, 40, 270 and 330 nm). The effective lifetimes shown are averaged over 5-10 wafers for each oxide thickness.

We interpret our experimental results of SiO<sub>2</sub> thickness dependence of both, the optimum final passivation quality after annealing as well as the required annealing time for achieving the optimum passivation, in terms of the hydrogen transport through the SiO<sub>2</sub> layer [7, 8]. Apart from a longer transport path through a thicker SiO<sub>2</sub> layer the transport of hydrogen through the SiO<sub>2</sub> can also be considered to be hampered by the larger volume of the thick SiO<sub>2</sub> layer: The SiO<sub>2</sub> itself contains dangling bonds and thus a thicker SiO<sub>2</sub> layer consumes a larger fraction of the hydrogen during its transport from the SiN through the oxide towards the Si/SiO<sub>2</sub> interface. Consequently, the chance for hydrogen atoms to reach the Si/SiO<sub>2</sub> interface becomes smaller when the oxide thickness increases and at the same time the duration for achieving final optimum interface passivation is prolonged (around 5 min annealing time for thin oxide and 10 min for thick oxide). Also, as the hydrogen stock in SiN is limited and, with time, more hydrogen is lost from the outer surface of the SiN film to the ambient, the obtainable final passivation quality decreases with increasing oxide thickness.

### Time stability of SiO<sub>2</sub>/SiN stack passivation

The stability of oxide passivation under various circumstances has been studied intensively, for example such as reported in references 9 and 10. Degradation of oxide passivation of boron-diffused surfaces has also been observed without particularly enforced impact from hydrogen, humidity or UV radiation [11-13], and recently degradation of oxide passivation without such degradation stimuli has also been reported for non-diffused surfaces [14].



**Figure 2** Time stability of passivation quality for *n*-type CZ silicon wafers (2.5 Ω cm) passivated with thermal-oxide/PECVD-SiN stack. The SRVs are shown for the best wafers of available oxide thickness set (10, 40, 270, 330 nm). Annealing made for 5 min at 400°C in air.

Here we report the oxide thickness dependence of the degradation of SiO<sub>2</sub>/SiN passivation stacks without intentional external degradation stimuli. Figure 2 shows the effective surface recombination  $S_{\text{eff,max}}$  for our best samples as determined from equation (1) after storage in the dark at room temperature. After 6 weeks of storage we have observed slightly decreasing effective lifetime for thick oxides (40 to 330 nm). 5 min of annealing at 400°C in air restores the passivation quality and it remains unchanged for the storage time of 35 weeks.

### CONCLUSIONS

The influence of the different SiO<sub>2</sub> thicknesses on surface passivation of *n*-type Cz silicon substrates by thermal-SiO<sub>2</sub>/PECVD-SiN stacks was investigated. An extended subsequent thermal annealing is necessary for thicker SiO<sub>2</sub> layers to obtain the optimum of surface passivation. We have found a clear correlation between the thickness of the oxide layers, the annealing duration and the absolute passivation quality of the samples. It was shown that an increase in SiO<sub>2</sub> thickness requires longer thermal annealing for achieving optimum passivation quality. Furthermore, the thicker SiO<sub>2</sub> layers in our SiO<sub>2</sub>/SiN stacks produce lower final passivation quality. We associate this effect with a hampered hydrogen transport from the SiN through the SiO<sub>2</sub> layer towards the Si/SiO<sub>2</sub> interface. The very low effective surface recombination velocities of less than 2.4 cm/s, achieved in our study, appear to be the best ever reported for the moderate resistivity (2.5 Ωcm) *n*-type Cz silicon wafers passivated by thermal-SiO<sub>2</sub>/PECVD-SiN stacks. This level of surface passivation is similar to that achievable by annealed thermal oxide [4]. We have also shown that during storage at room temperature in air the surface passivation by SiO<sub>2</sub>/SiN passivation does not degrade appreciably and that the passivation is particularly stable for thin oxides grown in a dry atmosphere.

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