

EFFECT OF SiN DEPOSITION TEMPERATURE ON SURFACE PASSIVATION OF N-TYPE CZ SILICON SUBSTRATES USING THERMAL-SiO₂/PECVD-SiN STACKS

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ABSTRACT: Improved surface passivation of 2.5 Ω cm *n*-type Cz silicon substrates by thermal-SiO₂/plasma-enhanced chemical vapour deposition SiN stacks is reported using low temperature (250-300°C) during the plasma-enhanced chemical vapour deposition of SiN. Low temperature SiN deposition leads to increasing the hydrogen content of the SiN layers. This improves the supply of hydrogen to the Si/SiO₂ interface and causes improved surface passivation. Surface recombination velocities lower than 2.4 cm/s for thick (270 nm) SiO₂/SiN stack are obtained by this method after post-deposition annealing at 400°C. The subsequent annealing is necessary for achieving optimum in passivation quality.

Keywords: Passivation, SiO₂, Stability

1 INTRODUCTION

The minimization of surface recombination losses is an important issue for improvements of a large variety of silicon-based microelectronic devices [1] and increasing the efficiency of silicon-wafer-based solar cells [2].

The surface passivation of crystalline silicon using thermally grown oxide or amorphous films based on hydrogenated silicon compounds has been the subject of intense research in recent years. Effective surface recombination velocities (SRV) in the range of 5-20 cm/s are typically shown in literature for *n*- and *p*-type high-resistivity (10-200 Ωcm) silicon for thin-film coatings with amorphous silicon [3], amorphous silicon nitride [4-8] and amorphous silicon carbide [9].

The surface passivation of as-grown thermal oxide is moderate, but is significantly improved by a subsequent annealing in forming gas (H₂ in N₂) [10] or upon depositing hydrogen-rich silicon nitride (SiN) layer onto the oxidised surface [6,7]. Recently, in [11], it was experimentally demonstrated that thin thermal-SiO₂/SiN stacks with subsequent thermal annealing give very good surface passivation ($S_{\text{eff}} \leq 2.4$ cm/s on *n*-type *c*-Si) due to a hydrogen transport from the SiN through the SiO₂ layer toward the Si/SiO₂ interface, activated by an annealing step. This passivation quality is comparable with the so-called *alnear* scheme [12], where a layer of Al is evaporated on the SiO₂ film prior to annealing at approximately 400°C. The aluminium reduces residual H₂O molecules in the SiO₂, which releases atomic hydrogen that eventually saturates dangling bonds at the Si/SiO₂ interface.

In this paper we report further improvement in passivation quality of SiO₂/SiN stacks by decreasing PECVD-SiN deposition temperature. The high quality of the Si/SiO₂ interface, which is grown into the silicon crystal at high temperature, and the subsequent very effective hydrogenation of dangling bond interface states during the SiN deposition and annealing play an important role in this process. The total hydrogen content in the SiN film decreases with increasing deposition temperature [13,14] due to the high mobility of hydrogen atoms. Therefore it is possible to increase the hydrogen content of the SiN layers by decreasing their deposition

temperature. The increased hydrogen content can lead to an improved supply of hydrogen to the Si/SiO₂ interface during the post-deposition annealing and thus to improved surface passivation.

2 EXPERIMENT DESCRIPTION

2.1 Preparing the samples

We use (100)-oriented Cz *n*-type silicon of 2.5 Ω cm resistivity and a thickness of 150 to 170 μm after saw-damage etching in KOH. Subsequently, the wafers were cleaned using the standard RCA procedure prior to oxidation in a cleaned quartz furnace tube at high temperatures. Our wafers were oxidized at 900 °C in wet O₂/H₂ ambient for 185 min, yielding 270 nm oxide thickness. It is known that the as-grown oxides give a very poor surface passivation and an increase in passivation quality is observed after hydrogen-rich PECVD-SiN deposition [6]. We have deposited 70 nm thick SiN films onto both surfaces of each wafer in a remote PECVD reactor. For these depositions we used substrate temperatures of 250 °C and 400 °C. Subsequently we annealed the wafers in ambient air at 350 °C or 400 °C on a hotplate for up to 150 min.

The effective lifetime τ_{eff} was measured by the quasi steady-state photoconductance and transient photoconductance decay techniques [15]. Both methods show excellent agreement in lifetime measurements. We assume infinite bulk lifetime for calculating the upper limits to the effective SRV $S_{\text{eff,max}}$ [16]:

$$S_{\text{eff,max}} \leq W / \tau_{\text{eff}} \quad (1)$$

where W is the wafer thickness.

2.2 Annealing of SiO₂/SiN stacks

Figure 1 shows the effective lifetime versus annealing time in air for *n*-type Cz silicon wafers (2.5 Ω cm), passivated with thick (270nm) thermal (wet) SiO₂/PECVD-SiN stack. The SiN films of these samples were deposited at substrate temperatures 250°C (solid symbols) and 400 °C (open symbols). After SiN deposition we measure the carrier lifetime of the wafers and subsequently anneal them in ambient air at 350°C

(circles) or 400°C (triangles) on a hotplate. After some minutes of annealing we take the wafer from the hotplate, let them cool down and measure again the effective carrier lifetime. We continue with this stepwise annealing until we observe saturation of the carrier lifetime. We find that lower annealing temperatures require prolonged annealing durations for obtaining a certain level of surface passivation for both, SiN deposited at 250°C or at 400°C. Furthermore, the required annealing duration for achieving a certain level of surface passivation is shorter in case of lower SiN deposition: 350°C annealing of the SiN deposited at 400°C achieves an optimum surface passivation after about 120 minutes, while the same annealing step applied to the low-temperature SiN (deposited at 250°C) achieves the final optimum already after 60 minutes of annealing. The most important finding is that the highest quality of surface passivation of SiO₂/SiN stacks is achieved for low SiN deposition temperatures. We associate this effect with the fact that SiN deposited at lower temperatures contains more hydrogen, which in return constitutes a larger supply of hydrogen for passivating dangling bonds at the Si/SiO₂ interface [13,14].

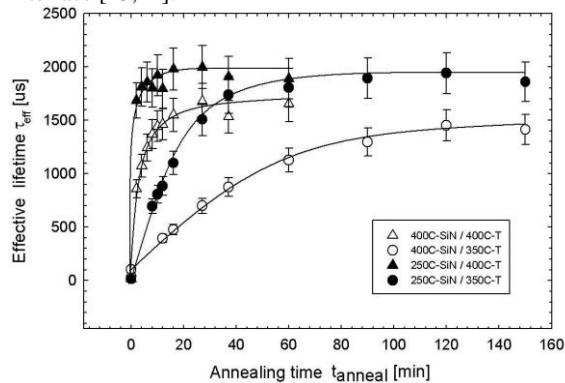


Figure 1: Effective lifetime, measured at injection level $\Delta n=1 \cdot 10^{15} \text{ cm}^{-3}$, versus annealing time in air for *n*-type Cz silicon wafers (2.5 $\Omega \text{ cm}$) passivated with thermal-SiO₂/PECVD-SiN stack. Different curves correspond to the different SiN deposition temperatures (250°C and 400°C) and annealing temperature (350°C and 400°C). The effective lifetimes shown are averaged over 10 samples of each experimental set. Error bars are determined by the quasi steady-state photoconductance measurements.

2.3 Time stability of SiO₂/SiN passivation

The stability of oxide passivation under various circumstances has been studied intensively, for example such as reported in references 17-22. In [12] we have shown the time stability of SiO₂/SiN passivation for different oxide thickness values without intentional external degradation stimuli. Here we report the stability in passivation quality of SiO₂/SiN stacks made at different SiN deposition temperatures.

Figure 2 shows the time stability of passivation quality for the best wafers from each experiment set. After 5 weeks of storage in the dark at room temperature we have observed slightly decreasing effective lifetime. 5 min of annealing at 350/400°C respectively restore the passivation quality, which remains unchanged for the subsequent storage time of 35 weeks. This stabilized passivation quality after the intermediate anneal after 8 weeks is contrary to typical expectation. The anneal after

8 weeks of storage restores the passivation quality to a degree very similar to the initial quality. However, the absence of subsequent degradation suggests that the sample may be in a different state than after the initial anneal.

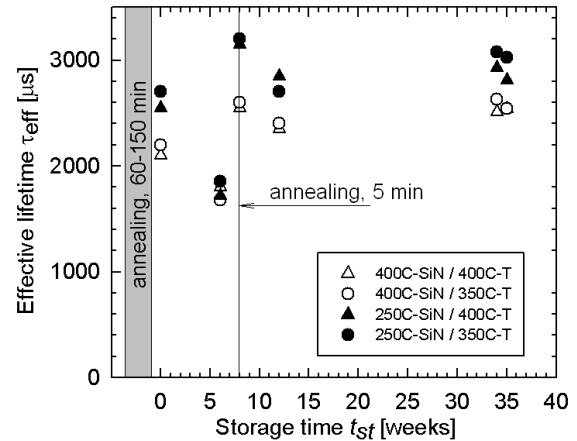


Figure 2: Time stability of passivation quality for *n*-type Cz silicon wafers (2.5 $\Omega \text{ cm}$) passivated with thermal-oxide/PECVD-SiN stack. Different points correspond to the different deposition temperatures (250°C and 400°C) and annealing temperature (350°C and 400°C). The effective lifetimes are shown for the best wafers of each experiment set.

3 CONCLUSIONS

In conclusion, the passivation quality of *n*-type Cz silicon substrates using thermal-SiO₂/PECVD-SiN stack systems is improved by decreasing the temperature during the plasma-enhanced chemical vapour deposition of SiN. We associate this effect with increasing the total hydrogen content in SiN film deposited at low temperatures. The subsequent annealing at high temperature (for instance, 400°C) is necessary for achieving the optimum in passivation quality.

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