

DETERMINING THE BULK LIFETIME OF UNPASSIVATED MULTICRYSTALLINE SILICON WAFERS

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ABSTRACT: The determination of the bulk lifetime of bare multicrystalline silicon wafers without the need of surface passivation is a desirable goal. The implementation of an in-line carrier lifetime analysis is only of benefit if the measurements can be done on bare unprocessed wafers and if the measured effective lifetime is clearly related to the bulk lifetime of the wafer. In this work we present a detailed experimental study demonstrating the relationship between the effective carrier lifetime of unpassivated wafers and their bulk carrier lifetime. Numerical modelling using the device simulation program PC1D is used to describe this relationship for different surface conditions taking into account the impact of a saw damage layers with poor electronic quality. Our results show that a prediction of the bulk lifetime from quasi-steady state photo conductance (QSSPC) carrier lifetime measurements on bare wafers is possible. Based on these results we suggest a simple procedure to implement the analysis for in-line inspection. Furthermore, we examine the relation between the effective lifetime of the bare, unprocessed wafers and the energy conversion efficiencies of solar cells made from neighboring wafers and find a clear correlation independent of the wafer position in the multicrystalline block.

Keywords: QSSPC, lifetime, bare, multicrystalline, silicon

1 INTRODUCTION

A wafer-based silicon solar cells production usually starts with an inspection of the incoming as-cut wafers. Present wafer inspection systems are designed to test the basic wafer properties such as geometry, contour integrity, thickness and resistivity. The next step towards a complete wafer characterization is the measurement of the bulk carrier lifetime. However, this is only of benefit if the measurements can be done on bare unprocessed wafers and if the measured effective lifetime is clearly related to the bulk lifetime of the wafer. As has been pointed out by Bentzen et al. [1], necessity for a detailed analysis of the electronic quality of multicrystalline wafers arises from the pressure to reduce production cost. Less than perfect feedstock material and fast solidification techniques often result in an enhanced formation of crystal imperfection and the contamination with transition metals. First experimental evidence that a combination of in-line quasi-steady-state photo conductance (QSSPC) measurements carried out under different injection densities is capable in reducing the number of wafers resulting in low energy conversion efficiencies has been presented by Enjalbert et al. [2]. In order to demonstrate the full potential and benefit of carrier lifetime measurements on unprocessed bare wafers, Sinton et al. [3] presented a methodology for measuring unprocessed, bare wafers using the QSSPC technique in order to determine the bulk lifetime. The aim of this work is to test this methodology for the use of multicrystalline silicon wafers. Therefore, we present a detailed experimental study demonstrating the relationship between the effective carrier lifetime of unpassivated wafers and their bulk carrier lifetime. In the first part of this paper numerical modelling using the device simulation program PC1D [4] is used to study the relationship between the bulk carrier lifetime and the effective carrier lifetime of bare wafers. We investigate the impact of the surface recombination velocity and take into account the impact of a saw damage layers with poor electronic quality. The second part shows the result of QSSPC carrier lifetime measurements on multicrystalline silicon wafers before and after saw damage removal. Finally, the relation of the effective

lifetime measured on unprocessed, bare wafers and the energy conversion efficiencies of solar cells made from neighbouring wafers is examined.

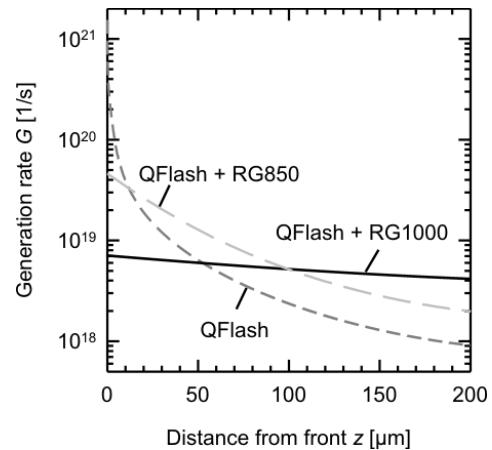


Fig. 1: Photogeneration profiles for a 200µm thick silicon wafer using a Quantum photo flash in combination with a Schott glass RG850 and RG1000 optical long pass filter.

Solving the continuity equation for perfectly uniform photogeneration and infinite surface recombination velocity, the relation between the actual bulk lifetime τ_b and the measured effective lifetime τ_{eff} is given by

$$\tau_{\text{eff}} = \tau_b \left(1 - \frac{2L}{W_w} \tanh\left(\frac{W_w}{2L}\right) \right) \quad (1)$$

where L is the diffusion length, and W_w is the wafer thickness. Using a Quantum xenon flash in combination with an infrared (IR) long pass filter the experimental photogeneration conditions are adapted to come close to the ideal case of uniform photogeneration. Even though a Schott glass RG1000 IR long pass filter would result in a more uniform photogeneration we use a 3 mm thick

Schott glass RG850 IR long pass filter. The advantage of this configuration is a higher photon flux and a reduced sensitivity to thickness variations from wafer to wafer as well as to optical properties of the wafer backside such as reflection and scattering. With decreasing wafer thickness the optical properties of the backside become increasingly important. An illustration of the different photogeneration profiles for a 200 μm thick wafer is shown in Fig. 1. In order to account for the real experimental conditions PC1D simulations are carried out. We investigate two different cases. In the first case the recombination at the surface is described by the surface recombination velocity S while in the second case the impact of a saw damage layer of finite thickness with poor electronic quality is considered. For both cases the input parameters for the simulation are the wafer thickness W_w , the wafer resistivity ρ and the bulk carrier lifetime τ_b (using $\tau_n = \tau_p$ and $E_t = 0$ eV). In the first case only one device region is necessary, whereas in the second case, we use three device regions, keeping the total thickness constant. For the first and third region each having a thickness W_d the bulk lifetime is set to 1 ns while all other parameters are kept the same as for the bulk region. Expected values for the unpassivated surfaces are ranging from 10^4 to 10^5 cm/s. A typical saw damage layer has a thickness between 2 and 15 μm . The output parameter from PC1D are the cumulative excess conductivity $\Delta\sigma_{\text{cum}}$, the electron and hole mobilities μ_n and μ_p as well as the photogeneration rate G . The effective carrier lifetime which would be measured by QSSPC is calculated according to

$$\tau_{\text{eff}} = \frac{\Delta n_{\text{av}}}{G} = \frac{\Delta\sigma_{\text{cum}}}{Gq(\mu_n + \mu_p)W_w} \quad (2)$$

The relation between the bulk and the effective lifetime resulting from the PC1D simulations are shown in Fig. 2. Aiming at a prediction of the bulk lifetime from the effective lifetime we identify three characteristic segments. In the first segment for very small effective carrier lifetimes the bulk recombination limits the effective carrier lifetime. The slope in the curve is small and the uncertainty in the measured effective lifetime additionally hampers a correct prediction of the bulk lifetime. In the second segment the slope of the curve increases and τ_b is clearly related to τ_{eff} . The third segment is characterized by the asymptotic value of the effective carrier lifetime defined by the strength of the surface recombination velocity. This asymptotic value shifts to smaller values with increasing surface recombination velocity until the kinetic limit is reached at $S \approx 2 \times 10^5$ cm/s. The incorporation of a saw damage layer results in an even more pronounced shift in the asymptotic value which is very sensitive to the damage layer thickness.

3 EXPERIMENTAL RESULTS

For the experimental verification of the methodology we carry out QSSPC measurements on multicrystalline silicon wafers before and after saw damage removal using a WCT-100 Sinton lifetime tester. In the QSS mode the effective carrier lifetime can be determined with an accuracy of approximately 10% [5]. All measurements are

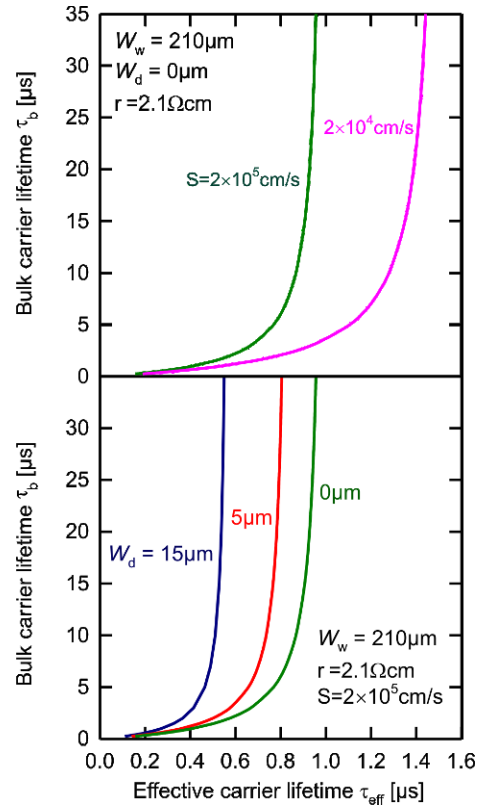


Fig. 2: Results of numerical device simulations using PC1D illustrating the relation between the effective carrier lifetime τ_{eff} of bare silicon wafers and the corresponding bulk carrier lifetime τ_b taking into account different surface recombination velocities (top) as well as the impact of a saw damage layer of poor electron quality (bottom). For all calculations the measured flash light spectrum in combination with a Schott glass RG850 infrared long pass filter is used as light source.

performed at an injection density Δn of $4 \times 10^{14} \text{ cm}^{-3}$. A higher injection density is difficult to obtain on bare wafers. At lower injection densities the lifetime might already be affected by trapping artefacts. Trapping of excess carriers may result in anomalously high apparent lifetimes when using photoconductance-based measurement techniques to determine recombination lifetimes [6]. To correct for potential trapping effects an analytical mathematical bias light correction procedure as suggested in Ref. 7 is performed on all measurements. In none of the measurements a change in the recombination lifetime is observed indicating that trapping is negligible at the injection density used throughout this study. The wafers were taken from defined positions of a multicrystalline block from bottom to top. Since the lifetime is expected to be lower in the bottom and top regions, more wafers were taken from these regions. All measurements are performed at the centre of the wafers averaging over an area of approximately 6 cm^2 . Measuring randomly chosen wafers from all three ingot regions at five positions covering the whole wafer area we found that the centre area is a representative mean for the whole wafer. Fig. 3 shows the results of the measurements carried out on a) bare as-cut wafers, b) the same wafers after etching away 30 μm of silicon in total using a KOH solution and c) after surface passivation of the same wafers with silicon

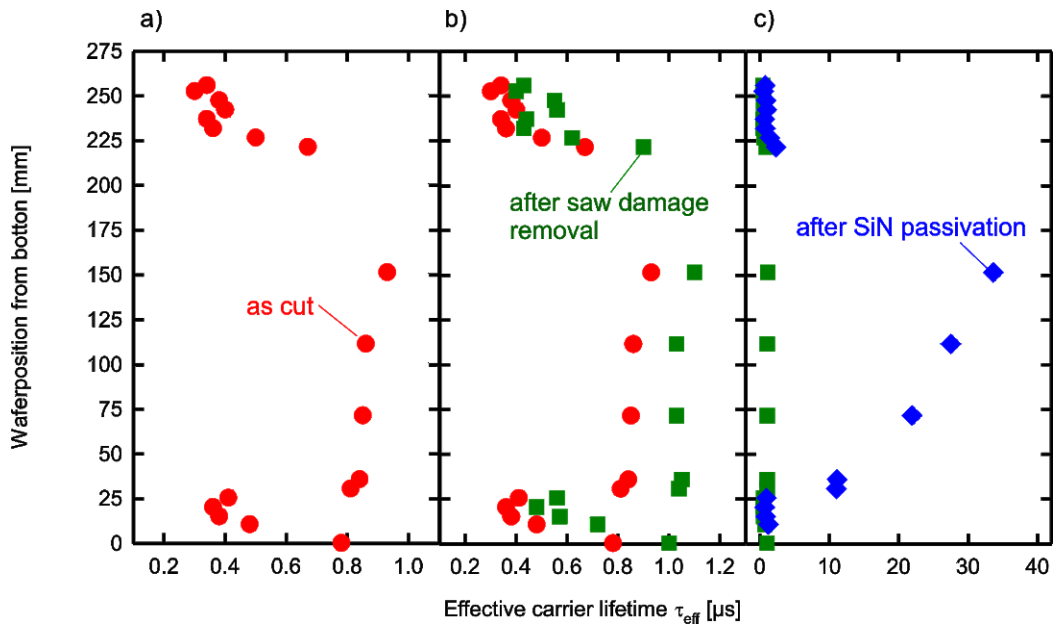


Fig. 3: Effective carrier lifetime determined from QSSPC measurements at an excess carrier density of Δn of $4 \times 10^{14} \text{ cm}^{-3}$ on bare as-cut wafers a), the same wafers after etching away 30 μm of silicon in total using a KOH solution b) and after surface passivation of the etched wafers with silicon nitride c).

nitride c). The surface recombination velocity from the nitride passivation is well below 5 cm/s [8] and ensures that the effective carrier lifetime is equal to the bulk carrier lifetime for values below 200 μs [9,10]. As expected from the literature [2,3,11,12] the carrier lifetime in the top and bottom regions of the ingot investigated is indeed smaller compared to that of the centre region. This trend is already visible in the as-cut data but becomes more pronounced after etching and especially after surface passivation. Since all lifetime values after surface passivation are below 200 μs , these values can safely be set to be equal to the bulk carrier lifetime. In Fig. 4 a) and b) the data sets of τ_b versus τ_{eff} for the as-cut and damage etched wafers, respectively, are shown as symbols. The lines represent PC1D simulation. Since the variations in the base resistivity ($2.1 \pm 0.2 \Omega\text{cm}$) over the whole ingot and the wafer thickness ($212 \pm 4 \mu\text{m}$ before and $184 \pm 5 \mu\text{m}$ after saw damage removal) is fairly small, we use the average values of the base resistivity and the thickness for the PC1D simulations. As can be seen for the as-cut case in Fig. 4 a), we have to introduce a damage layer of approximately 2.5 μm to both surfaces to fit the data set adequately. A diffusion limited surface recombination ($S \approx 2 \times 10^5 \text{ cm/s}$) does not satisfyingly describe the relation. As shown in Fig. 5, tests of as-cut wafers from various suppliers confirmed this result. Note that in general the thickness of the saw damage layer critically depends on the sawing conditions and might therefore be different for different suppliers or saws used for wafering. After saw damage removal a diffusion limited surface recombination underestimates the surface quality. A limited surface recombination velocity of $2 \times 10^4 \text{ cm/s}$ results in the best modelling of the experimental data. This value is well below the kinetic limit and consistent with values published by Mäckel et al. [13] for bare wafers with polished or shiny etched surfaces. Our results show that a prediction of the bulk lifetime from measurements on

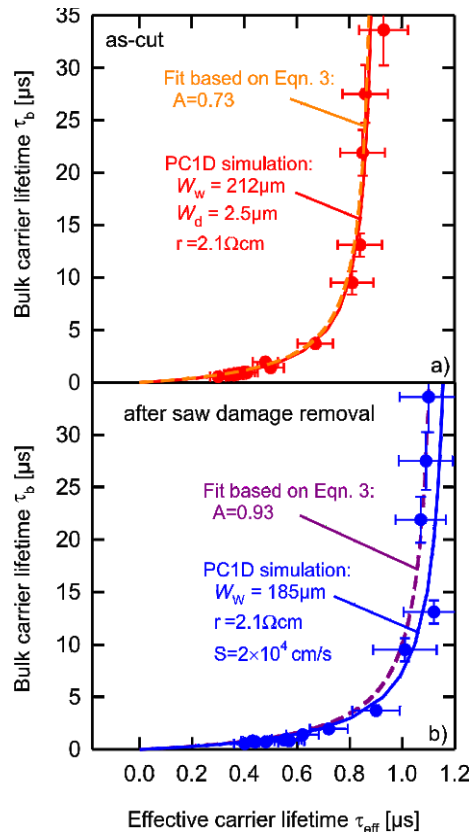


Fig 4: Experimental data of the bulk carrier lifetime as a function of the effective carrier lifetime for as-cut wafers a) and after saw damage removal b). While the relation for the as-cut case can best be modelled introducing a saw damage layer of thickness $W_d = 2.5 \mu\text{m}$ to both surfaces (5 μm in total) the best fit after saw damage removal is obtained for a surface recombination velocity of $2 \times 10^4 \text{ cm/s}$.

bare wafers is possible. However, our results also indicate, that the thickness of the saw damage layer is a critical parameter. Thus, the saw damage depth should be determined or removed prior to the lifetime measurement.

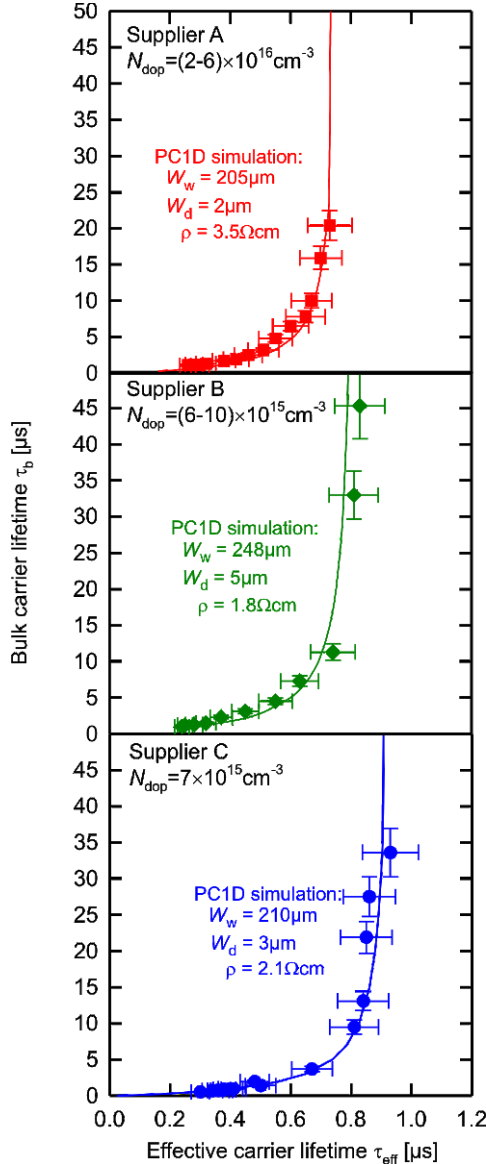


Fig 5: Experimental data of the bulk carrier lifetime as a function of the effective carrier lifetime for as-cut wafers of three different suppliers. Saw damage layers between 2 and 5 μm need to be assumed for best modelling of the data.

4 APPLICATION TO IN-LINE MEASUREMENTS

In order to transfer this type of analysis into a production line one would like to avoid numerical modelling in order to find the vertical asymptote as a measure of the surface recombination. As has been shown in Ref. 3, the numerically-derived results can be fit with a modified version of Eqn. 1

$$\tau_{\text{eff}} = A\tau_b \left(1 - \frac{2L}{W_w} \tanh\left(\frac{W_w}{2L}\right) \right) \quad (3)$$

where A is a fit parameter defining the position of the vertical asymptote. As shown in Fig. 4 Eqn. 3 can also be used to fit the experimental data by adjusting the fit parameter A . The procedure for the in-line application would be to continuously measure the effective carrier lifetime and to keep a running average of the highest measured lifetimes. One might, for example, use the top 5% of the carrier lifetimes measured on the last 500 to 1000 wafers. This average of the top lifetime values defines the position of the asymptote and the parameter A is continuously adapted to fit this asymptote. By this approach all other bulk lifetime values can be determined quite accurately from the measured effective carrier lifetime. For the determination of A in Fig. 4 we used the top 3 effective carrier lifetime values. An assumption of this approach of course is that among the distribution of wafers within each batch tested is reasonably broad and contains at least a few wafers of sufficiently good quality to define the asymptote.

5 RELATION TO SOLAR CELL ENERGY CONVERSION EFFICIENCY

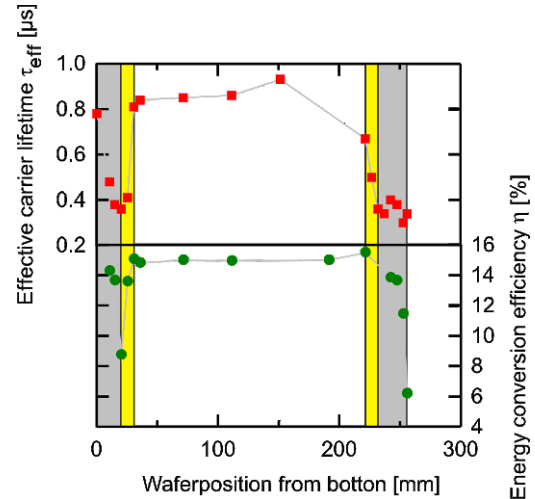


Fig 6: Measured effective carrier lifetime of bar as cut wafers and energy conversion efficiency of industrial screen printed solar cells processed on neighbouring wafers as a function of the wafer position within a multicrystalline silicon brick. Top and bottom regions are marked gray, transitions regions are marked yellow.

The remaining question most important to solar cell manufacturers is if it is possible to define a lower effective carrier lifetime limit to sort out wafers intended to result in solar cells with reduced energy conversion efficiency. This situation is far more complex since the carrier lifetime might improve or degrade considerably within the solar cell process depending on the impurities and crystal defects present in the wafer. Since a detailed study monitoring the change of the recombination activity throughout the complete solar cell production process is far beyond the scope of this paper. For this reason, we confine ourselves to the comparison of the effective carrier lifetime measured on bare as-cut wafers with the characteristic parameters of $156 \times 156 \text{ mm}^2$ screen printed industrial type solar cells processed from neighbouring wafers.

As can be seen from Fig. 6, samples from the centre part of the brick show the highest lifetime values while a decrease towards the bottom and top is observed. Qualitatively, all solar cell parameters follow this trend. Even though only a weak correlation is found between the effective carrier lifetime measured on the as-cut wafers and the open-circuit voltage of the cells, plotting the energy conversion efficiency as a function of the effective carrier lifetime as done in Fig. 7 allows to define a lower lifetime limit as criteria for sorting out wafers prior to the solar cell manufacturing process which will result in low energy conversion efficiency.

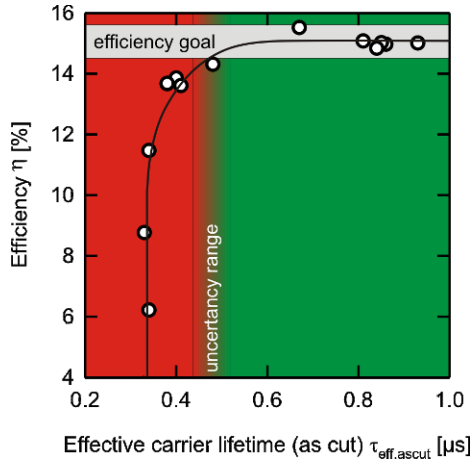


Fig. 7: Measured energy conversion efficiency as a function of the measured effective as-cut carrier lifetime. In the present case, the correlation between the two parameters allows defining a lower carrier lifetime limit to reject wafers intended to yield low energy conversion efficiencies.

Aiming at an efficiency of $15.0 \pm 0.5\%$ in the present case one would sort out all wafers with an effective lifetime below $0.4 \mu\text{s}$. One might argue that this finding is not representative since metallic impurities which might be gettered during the solar cell process and crystallographic defects which tend to be less affected by the solar cell process would both result in a low lifetime but in different energy conversion efficiencies.

On the basis of the present data we cannot yet invalidate this argument totally. However, own investigations on a larger number of cells (not shown here) as well as the results of Ref. 14 allow concluding that this argument only holds for so called “transition regions” located between the centre region and the bottom and top regions of a multicrystalline brick. In these transition regions both, crystal defects and impurities are present. However the impurity concentration is considerably smaller compared to the bottom and top regions and can thus be effectively gettered. The effective carrier lifetime in transition regions and the centre part are therefore limited by crystallographic defects which are in most cases intra-grain defects and in particular dislocation networks and cluster. These crystallographic defects effectively lower the luminescence emission and at the same time give rise to minority carrier trapping. For this reason a combined approach either taking account the area of tangled defects A_{TD} as described in Ref. 14 or the trap density proposed by Enjalbert et al. [2] may result in a better correlation

between wafer quality and solar cell energy conversion efficiency.

CONCLUSION

A methodology for the determination of the bulk lifetime from lifetime measurements on bare unpassivated samples has been tested for multicrystalline silicon wafers. With the use of numerical modelling, the correspondence between the measured effective carrier lifetime of bare wafers and their bulk lifetime is studied for different surface conditions. In the as-cut state the introduction of a surface-near damage layer of poor electronic quality was necessary to model the surface recombination adequately. The asymptotic lifetime value critically depends on the recombination properties of the surface and can thus be used to determine the effective depth of the saw damage. After saw damage removal best modelling of the experimental data was achieved for a surface recombination velocity of only $2 \times 10^4 \text{ cm/s}$ which is well below the kinetic limit. The experimental data did not only agree well with the predicted relation from device modelling but also with the prediction of a simple analytical description. Based on this analytical description a procedure to implement the carrier lifetime analysis for in-line inspection is introduced. The definition of a sorting criteria for wafers intended to become less efficient solar cells appears possible due to a correlation between the effective carrier lifetime and the energy conversion efficiency of industrial solar cells made from neighbouring wafers.

APPENDIX: Analytical solutions for the effective lifetime in the case of uniform photogeneration and infinite surface recombination velocities

As can be seen from Fig. A1, for infinite surface recombination, a significant or even a dominant, fraction of photogenerated carriers will flow towards the surface and recombine there. The recombination strength of the surface is characterized by the surface recombination velocity, S , which when multiplied by the excess carrier density gives the number of recombination events at the

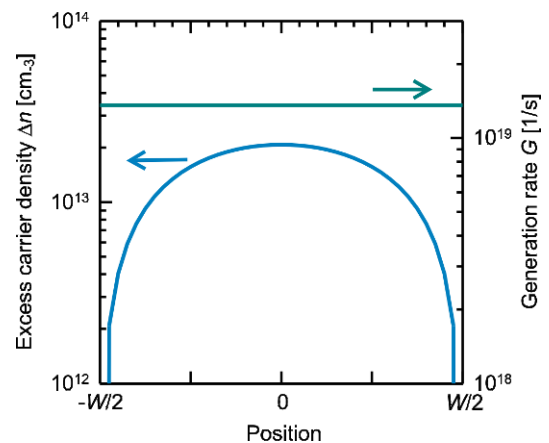


Fig. A1: Depth profile of the excess carrier concentration Δn for a sample of thickness W , uniform generation and infinite surface recombination S at $-W/2$ and $+W/2$, respectively.

surface per unit time. This number is precisely equal to the number of carriers flowing towards the surface. That is, we can state that the electron current density towards the surface is equal to the recombination rate at that surface:

$$J_n = -qD_n \left. \frac{dn}{dz} \right|_{z=W_w/2} = qS_n \Delta n(W_w/2) \quad (4)$$

The continuity equation in steady state for electrons in p -type silicon is:

$$0 = G - \frac{\Delta n}{\tau_n} + \frac{1}{q} \frac{dJ_n}{dz} \quad (5)$$

For infinite surface recombination velocity at both surfaces, $S=\infty$, the solution is:

$$\Delta n(z) = G\tau \left\{ 1 - \frac{\cosh\left(\frac{z}{L}\right)}{\cosh\left(\frac{W_w}{2L}\right)} \right\} \quad (6)$$

where L is the minority carrier diffusion length, defined as $L = \sqrt{D_n \tau_n}$.

The cumulative photoconductance follows by integrating the above expression (between $-W_w/2$ and $+W_w/2$) and multiplying by q and the sum of electron and hole mobilities, μ_n and μ_p , respectively:

$$\Delta\sigma_{cum} = G\tau \left(W - 2L \tanh\left(\frac{W_w}{2L}\right) \right) \cdot q \cdot (\mu_n + \mu_p) \quad (7)$$

Finally, the effective carrier lifetime (as measured by QSSPC) is given by:

$$\tau_{eff} = \frac{\Delta\sigma_{cum}}{Gq(\mu_n + \mu_p)W_w} = \tau \left(1 - \frac{2L}{W_w} \tanh\left(\frac{W_w}{2L}\right) \right). \quad (8)$$

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